

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-18. (Canceled).

19. (New) A system, comprising:

- a host bus to transfer at least one of information and instructions;
- a peripheral interface bus to interface to at least one peripheral;
- a processor arrangement coupled to the host bus, the processor arrangement including an execution unit to execute instructions;
- a main memory coupled to the host bus to store the instructions;
- a read-only-memory coupled to the host bus to store information for use by the processor arrangement;
- a bridge device to communicate information between the host bus and the peripheral interface bus, the bridge device including a multi-mode measurement arrangement to measure at least one of a metric and a performance parameter of the system, wherein the system is operable to perform the following steps:

- (a) providing one of a reference parameter and a next reference parameter;
- (b) receiving starting event information corresponding to a logic event, ending event information corresponding to the logic event, and at least one identification parameter information associated with the logic event;
- (c) determining an actual parameter corresponding to at least one of a duration parameter and a capacity parameter corresponding to the logic event;
- (d) comparing the actual parameter to the reference parameter and providing a comparison result; and
- (e) if the comparison result at least indicates that the actual parameter is no less than the reference parameter, performing at least one of replacing the reference parameter with the actual parameter to provide the next reference parameter and providing the at least one identification parameter.

20. (New) The system of claim 19, wherein the multi-mode measurement device is operable in an event-counting mode, an event-histogram mode, and a single event identification mode.

21. (New) The system of claim 19, wherein the peripheral interface bus includes a peripheral component interconnect (PCI) bus.

22. (New) The system of claim 19, wherein the at least one peripheral include a mass storage device coupled to the peripheral interface bus, and a data storage medium coupled to the mass storage device to store at least one of measurement data representation software and frequency distribution representation software.

23. (New) The system of claim 22, wherein the mass storage device includes a CD-ROM drive.

24. (New) The system of claim 22, wherein the data storage medium includes a compact disc read-only memory (CD-ROM).

25. (New) The system of claim 22, wherein the at least one of the measurement data representation software and the frequency distribution representation software include user interface software to interact with a user via an input device and a display device.

26. (New) The system of claim 19, further comprising:

an input device to receive input; and
a display device to display information.

27. (New) The system of claim 26, wherein the input device includes at least one of a keyboard and a cursor device.

28. (New) The system of claim 26, wherein the display device includes as least one of a monitor and a liquid crystal display.

29. (New) A method of determining an inter-arrival time distribution for a processor bus queue, comprising:

- (a) setting a bucket register to a minimum value of a maximum histogram bucket value;
- (b) using an active input arrival signal from the processor bus queue to reset and start a counter;
- (c) using an inactive input arrival signal from the processor bus queue to stop the counter and cause a comparing arrangement to compare a count for an event and a bucket register value, and to reset the counter; and
- (d) repeating steps (a) through (c) for each minimum bucket value.

30. (New) The method of claim 29, wherein the processor bus queue includes one of a processor bus transaction queue and a processor bus in-order-queue.

31. (New) The method of claim 29, wherein the processor bus queue includes a head of processor bus queue (HOPBQ).

32. (New) A method of identifying a maximum queue service time, comprising:

- using a first active output arrival signal to reset and start a counter;
- using a first active output departure signal to stop the counter and cause a comparing arrangement to compare a count for a first event and a time register value;
- latching in a first transfer address in an identifier latch arrangement;
- finding a cycle that occurs after a maximum buffer empty time; and
- using a head event of a queue blocking time to find the maximum queue service time.

33. (New) The method of claim 32, wherein the step of finding a cycle that occurs after a maximum buffer empty time includes:

- using a second active output departure signal to reset and start a second counter;

using a second active output arrival signal to stop the second counter and cause the comparing arrangement to compare a count for a second event and the time register value;
and

latching in a second transfer address in the identifier latch arrangement.

34. (New) The method of claim 32, wherein the second active output departure and arrival signals are associated with a processor bus transaction queue.